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J. Williams 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Joseph Williams
Case: 2
Serial No.: 10/023,127
Filing Date: December 17, 2001
Group: 2661
Examiner: To Be Assigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature: Alvise A. Glaser Date: January 6, 2003

Title: Mesh Architecture for Synchronous
Cross-Connects

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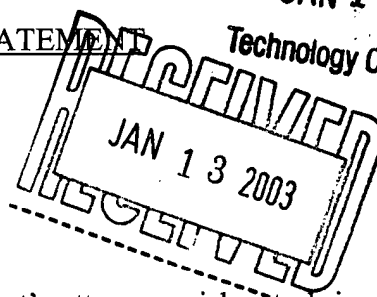
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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:



Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying Form PTO-1449. A copy of each listed document is enclosed.

1. C. Clos, "A Study of Non-Blocking Switching Networks," Bell Labs Technical Journal, pp. 406-424 (1952).

2. S. Kumar et al., "An Algorithm for Control of a Three Stage Clos-Type Interconnection Network," Fourth IEEE Region 10 International Conference, pp. 794-797 (1989).

3. C. Scheideler et al., "From Static to Dynamic Routing: Efficient Transformations of Store-and-Forward Protocols," *SIAM Journal on Computing*, Vol. 30, No. 4, pp. 1126-1155 (1999).

4. R. Cypher et al., "Universal Algorithms for Store-and-Forward and Wormhole Routing," *In Proc. of the 28th ACM Symp. on Theory of Computing (STOC)*, pp. 356-365 (1996).

5. J. Hopcroft et al., "An $n^{5/2}$ Algorithm for Maximum Matchings in Bipartite Graphs," *SIAM Journal of Computing*, Vol. 2, No. 4, pp. 225-231 (Dec. 1973).

6. H.N. Gabow et al., "Algorithms for Edge Coloring Bipartite Graphs and Multigraphs," *SIAM Journal of Computing*, Vol. 11, No. 1 (February 1982).

7. A. Schrijver, "Bipartite Edge Coloring in $O(\Delta m)$ Time," *SIAM Journal of Computing*, Vol. 28, No. 3, pp. 841-846 (Dec. 1973).

8. J. Carpinelli et al., "Applications of Edge-Coloring Algorithms to Routing on Parallel Computers," *Proceedings of the Third International Conference on Supercomputing*, Boston, MA, pp. 249-257 (May 1988).

It is believed that there is no fee due in conjunction with the filing of this Information Disclosure Statement. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Ryan, Mason & Lewis, LLP Deposit Account No. 50-0762** as required to correct the error.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,



Date: January 6, 2003

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FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT



Applicant(s): Joseph Williams
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U.S. PATENT DOCUMENTS

EXAMINER				FILING DATE	
INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER				TRANSLATION	
INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	YES NO

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OTHER DOCUMENTS

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EXAMINER		REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
INITIAL			

1. C. Clos, "A Study of Non-Blocking Switching Networks," Bell Labs Technical Journal, pp. 406-424 (1952).
2. S. Kumar et al., "An Algorithm for Control of a Three Stage Clos-Type Interconnection Network," Fourth IEEE Region 10 International Conference, pp. 794-797 (1989).
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Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.